EMBARGOED UNTIL FEB. 23, 2015, 4:45 PM PACIFIC U.S. TIME

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ISSCC 2015

"CARRIZO"

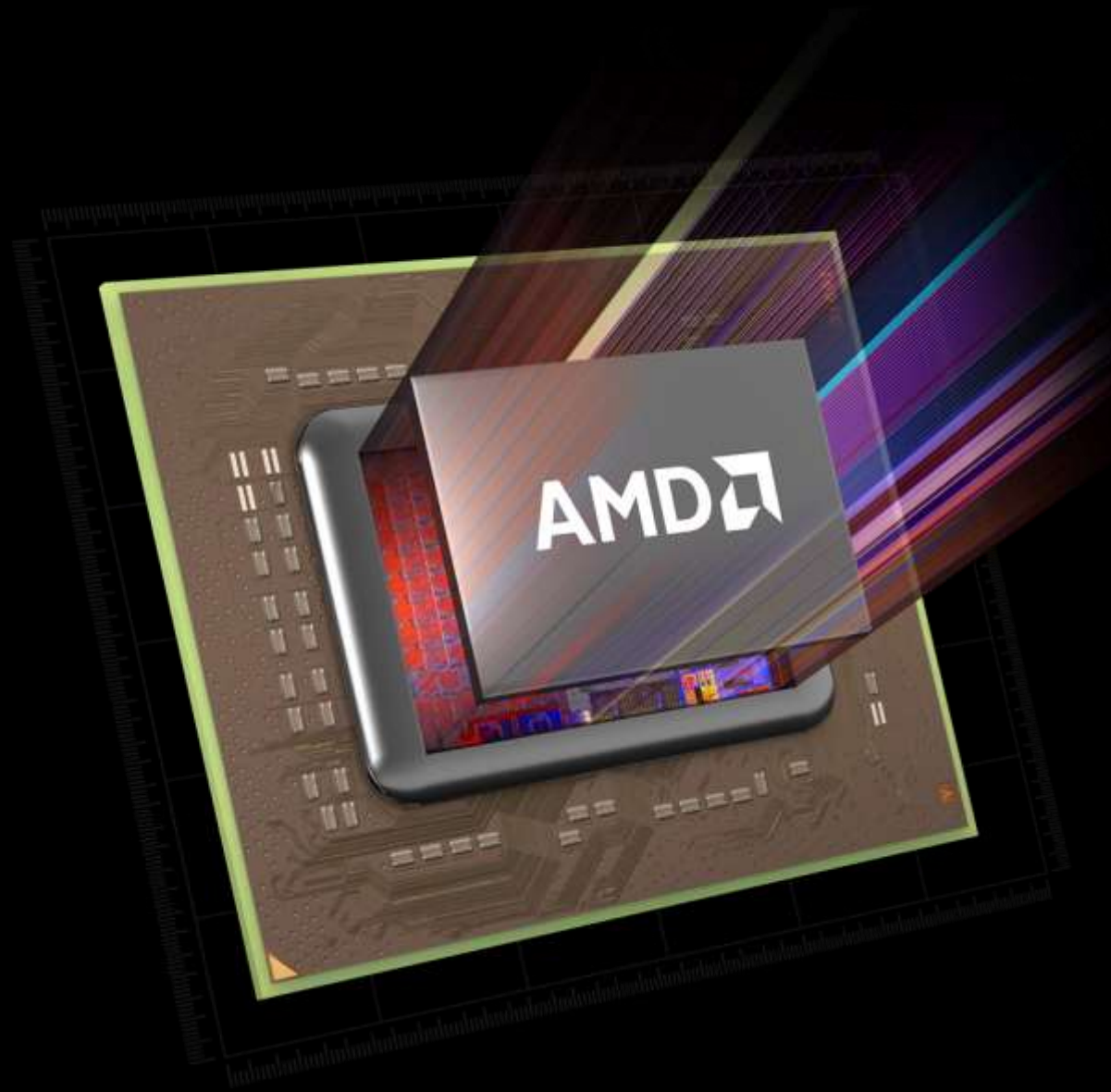
CAUTIONARY STATEMENT

The following presentation contains forward-looking statements concerning Advanced Micro Devices, Inc. (“AMD” or the “Company”) including, among other things: timing, availability, features and functionality of the AMD “Carrizo” APU, AMD “Carrizo –L” SoC; AMD’s ability to improve its energy efficiency technologies for its future products; AMD’s goal to improve energy efficiency for AMD mobile platforms by at least 25 times by 2020; and AMD’s goal to outpace historical energy efficiency trends, which are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act. Forward-looking statements are commonly identified by words such as "would," "may," "expects," "believes," "plans," "intends," "projects," and other terms with similar meaning. Investors are cautioned that the forward-looking statements in this press release are based on current beliefs, assumptions and expectations, speak only as of the date of this press release and involve risks and uncertainties that could cause actual results to differ materially from current expectations. Investors are cautioned that the forward-looking statements in this presentation are based on current beliefs, assumptions and expectations, speak only as of the date of this presentation and involve risks and uncertainties that could cause actual results to differ materially from current expectations. Risks include that Intel Corporation's pricing, marketing and rebating programs, product bundling, standard setting, new product introductions or other activities may negatively impact AMD’s plans; that AMD will require additional funding and may be unable to raise sufficient capital on favorable terms, or at all; that customers stop buying AMD’s products or materially reduce their operations or demand for AMD’s products; that AMD may be unable to develop, launch and ramp new products and technologies in the volumes that are required by the market at mature yields on a timely basis; that AMD’s third-party foundry suppliers will be unable to transition AMD’s products to advanced manufacturing process technologies in a timely and effective way or to manufacture AMD’s products on a timely basis in sufficient quantities and using competitive process technologies; that AMD will be unable to obtain sufficient manufacturing capacity or components to meet demand for its products or will not fully utilize its projected manufacturing capacity needs at GLOBALFOUNDRIES, Inc. (GF) microprocessor manufacturing facilities; that AMD’s requirements for wafers will be less than the fixed number of wafers that it agreed to purchase from GF or GF encounters problems that significantly reduce the number of functional die it receives from each wafer; that AMD is unable to successfully implement its long-term business strategy; that the completion and impact of the 2014 Restructuring Plan and AMD’s transformation initiatives could adversely affect AMD; that AMD inaccurately estimates the quantity or type of products that its customers will want in the future or will ultimately end up purchasing, resulting in excess or obsolete inventory; that AMD is unable to manage the risks related to the use of its third-party distributors and add-in-board (AIB) partners or offer the appropriate incentives to focus them on the sale of AMD’s products; that AMD may be unable to maintain the level of investment in research and development that is required to remain competitive; that there may be unexpected variations in market growth and demand for AMD’s products and technologies in light of the product mix that it may have available at any particular time; that global business and economic conditions will not improve or will worsen; that PC market conditions will not improve or will worsen; that PC market conditions will not improve or will worsen; that demand for computers will be lower than currently expected; and the effect of political or economic instability, domestically or internationally, on AMD’s sales or supply chain. Investors are urged to review in detail the risks and uncertainties in the Company's Securities and Exchange Commission filings, including but not limited to the Quarterly Report on Form 10-Q for the quarter ended September 27, 2014.

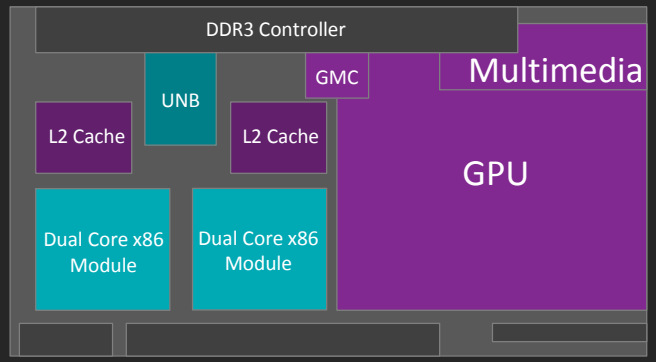
NEW PERFORMANCE MOBILE APU – “CARRIZO”

NEXT GENERATION PERFORMANCE APUs WITH FULL HSA CAPABILITY

- New “Excavator” core optimized for low power notebook/convertible form factors
- Next Generation AMD Radeon™ Graphics Core Next architecture with support for Mantle, DirectX® 12, and Dual Graphics
- Single-chip integration of the APU and the Southbridge onto a single die
- Significant performance and battery life improvements.
- First processor in the world with full HSA 1.0 support
- AMD Secure Processor, leveraging ARM® TrustZone technology for Enterprise-class security
- Single, scalable infrastructure shared with “Carrizo-L”

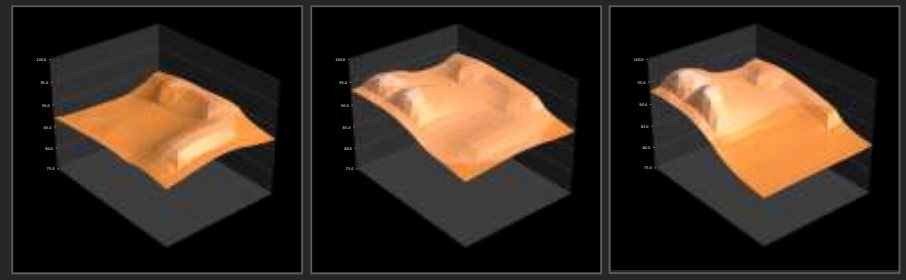


INTRINSIC ENERGY EFFICIENCY WITH ACCELERATED PROCESSORS (APU)

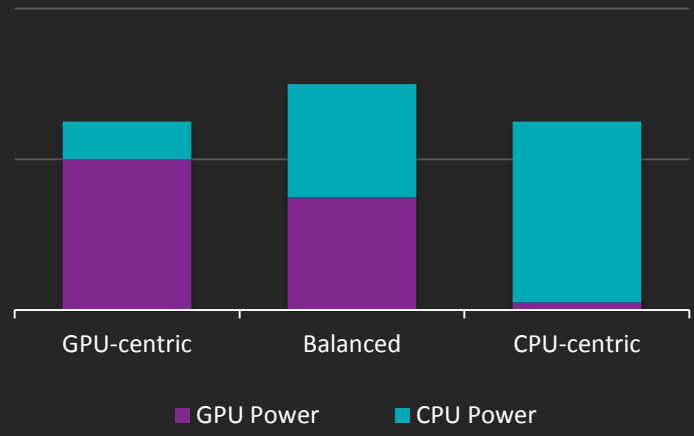


- Combines CPUs, GPU and multi-media accelerators on a single die
- APUs are optimized for greater efficiency
  - Efficient, fine-grained power management between CPU and GPU
  - CPU <-> GPU communication power dramatically reduced relative to separate chips
  - Shared memory interface helps save power

Temperature Distribution Plots



CPU <-> GPU Power Trading



AMD APU ENERGY EFFICIENCY WITH HSA

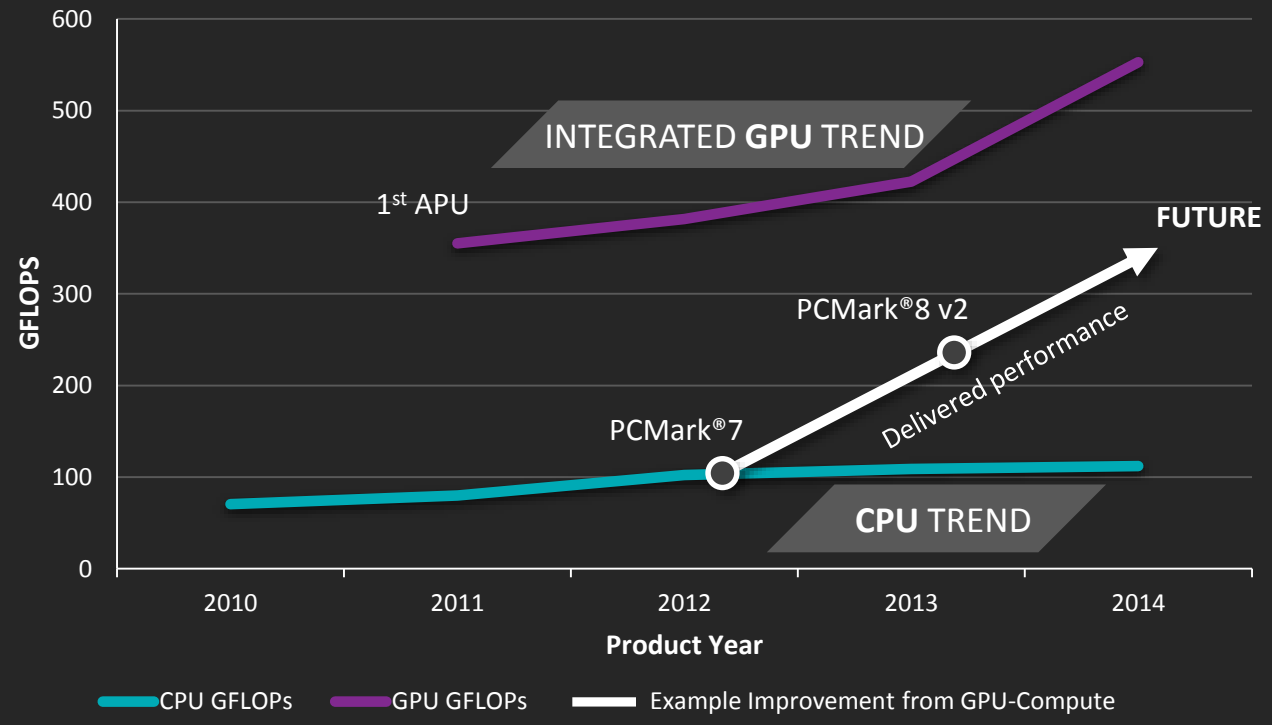
"CARRIZO" IS THE FIRST FULLY HSA COMPLIANT SOC

AMD

WHAT DOES THIS MEAN FOR POWER?

- Many workloads execute more efficiently using GPU compute resources rather than CPU only
  - E.g. video indexing, natural human interfaces, pattern recognition
- For the same power, much better performance: lower energy per operation → greater efficiency

COMPUTE CAPACITY TREND IN PCs

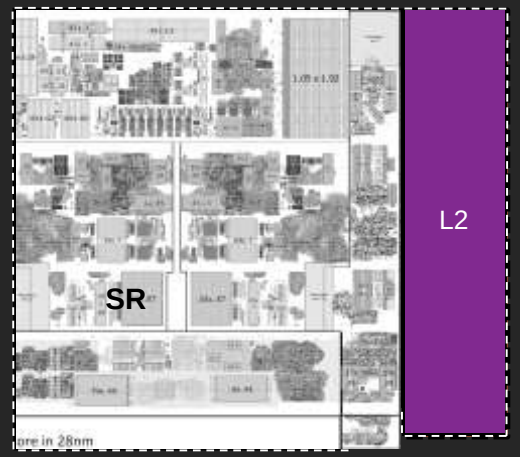


Source: AMD Internal data

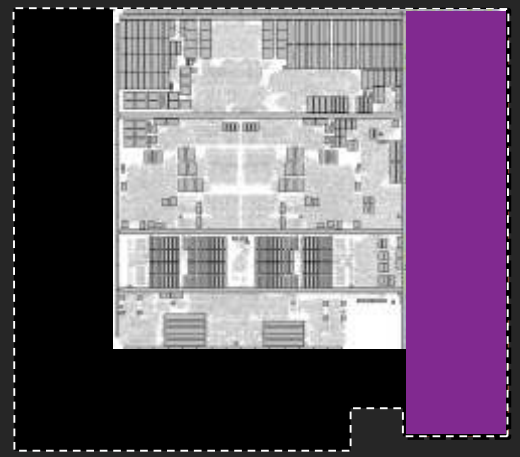
POWER OPTIMIZED CPU "EXCAVATOR" WITH HIGH DENSITY LIBRARY DESIGN

AMD

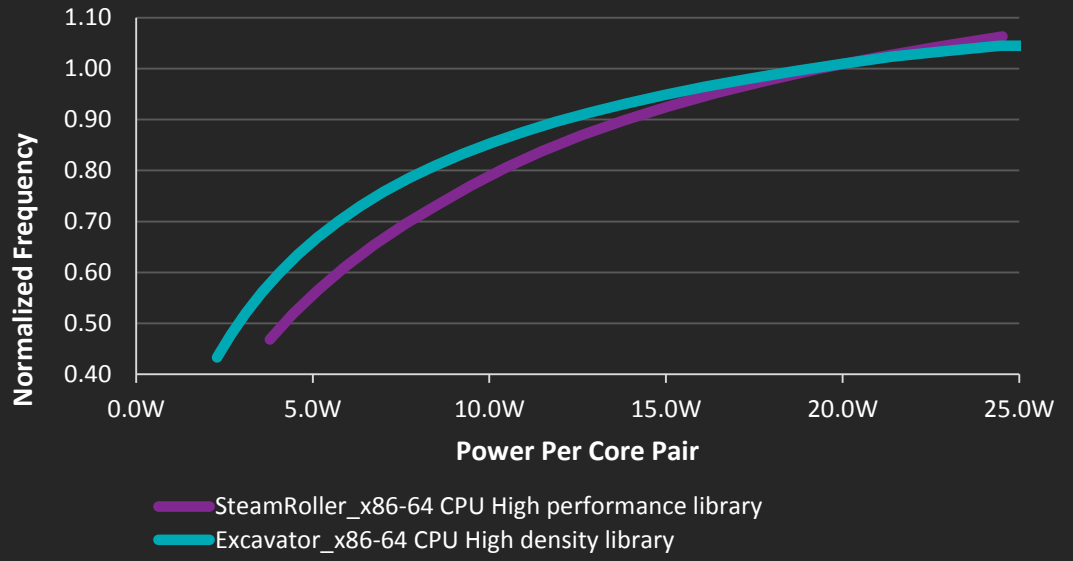
"Steamroller" Library Implementation



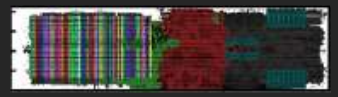
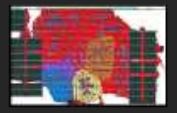
"Excavator" High-density Library Design



Achieves 23% area reduction, and lower power in the same 28nm technology node



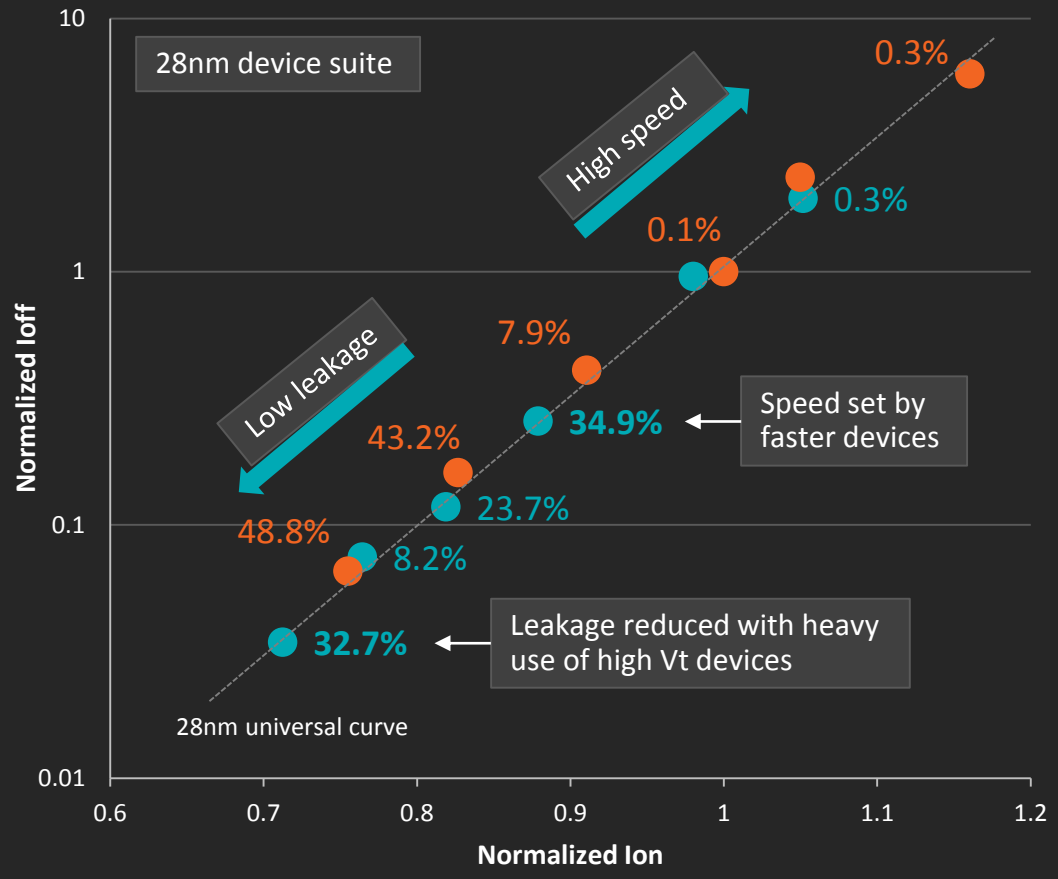
High Performance vs. High Density Cell Example

	HP Library	HD Library
Floating Point Scheduler 38%		
FMAC 35%		
I-Cache Control 35%		

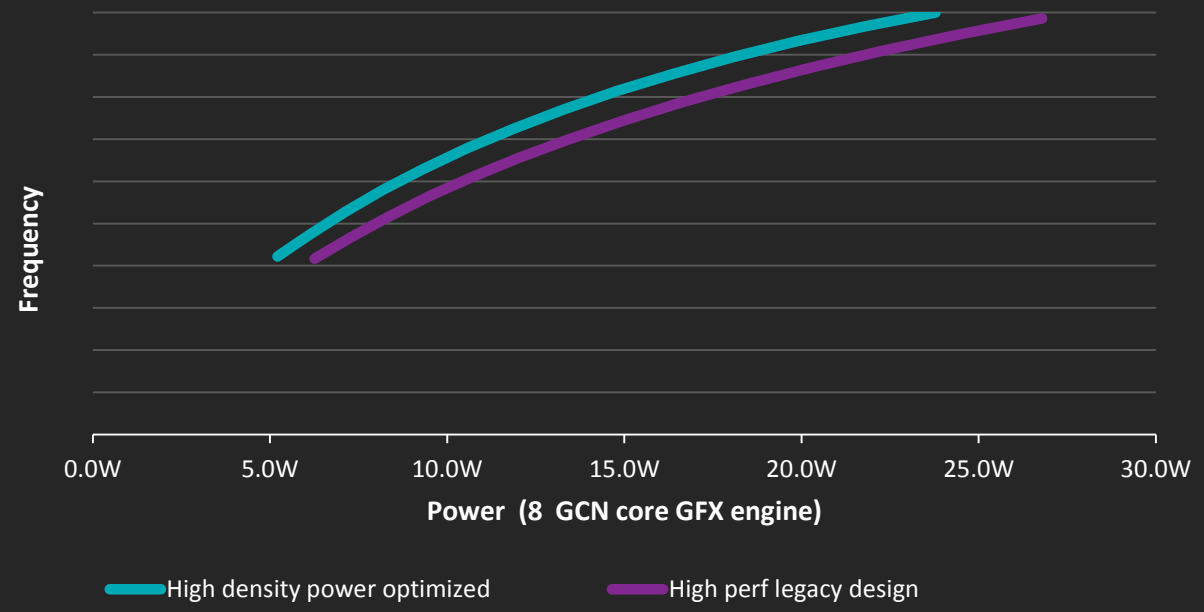
Prior generation CPU-centric tapered metal stack

General purpose GPU-oriented stack enables greater density

“CARRIZO” LOW POWER OPTIMIZED GRAPHICS



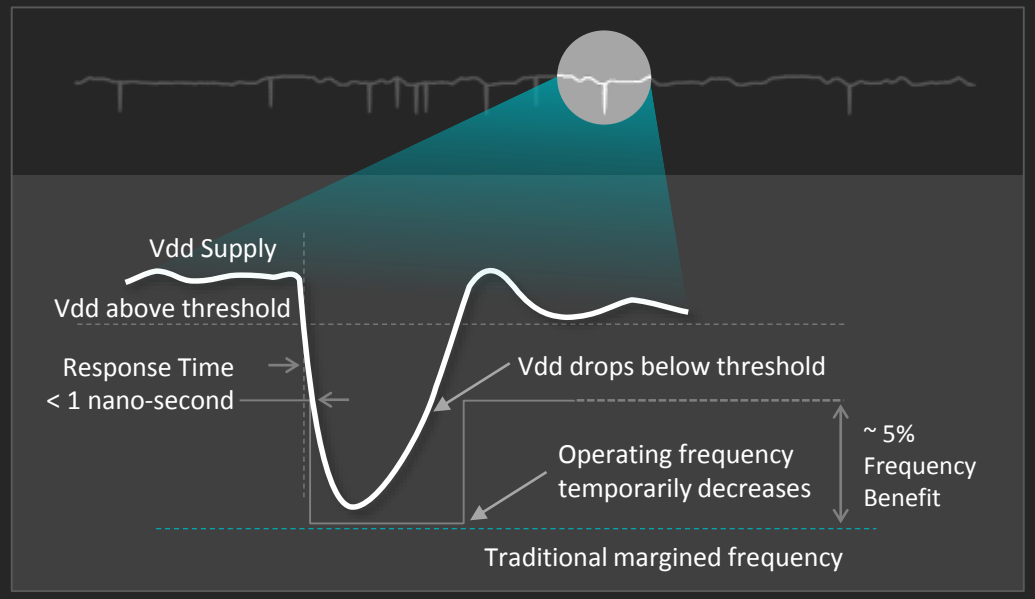
18% leakage reduction and timing with faster RVT devices enables 10% higher frequency at same power level, or up to 20% lower power at same frequency

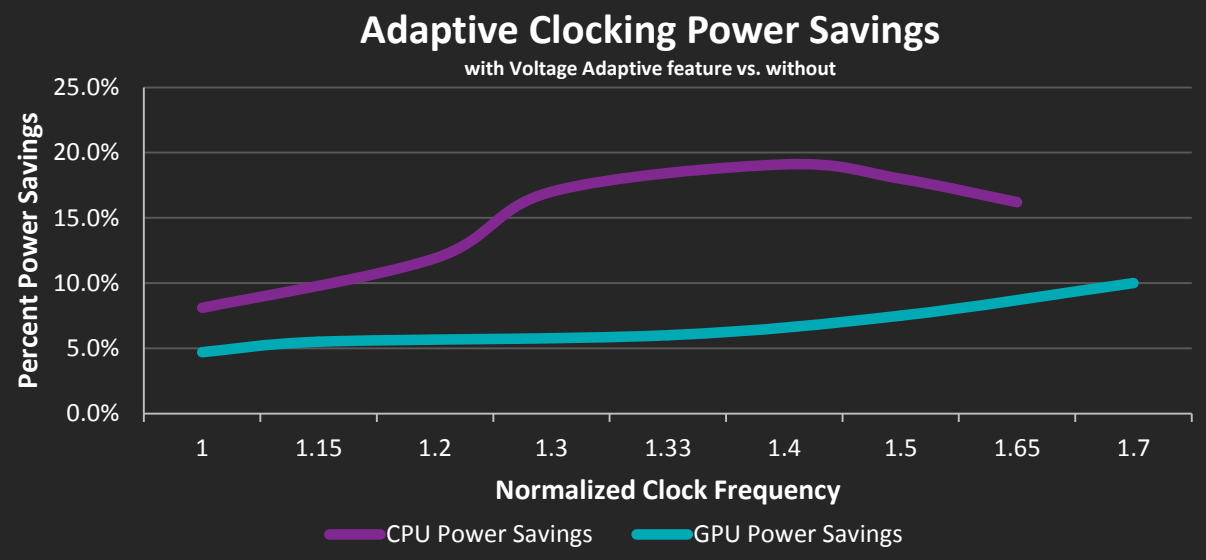


VOLTAGE ADAPTIVE OPERATION

- Delivering low noise voltage to high performance CPUs, GPUs and APUs has always been a challenge for the industry
- The variations that happen are typically about 10% of the nominal value – that means at least 20% power is wasted covering these voltage variations (power goes as the square of voltage)
- AMD's unique voltage adaptation feature recovers much of that wasted power by operating at the average voltage and quickly reducing frequency for the brief periods when the voltage reduces

Voltage adaptive feature applied to both CPU and GPU in "Carrizo" results in 19% and 10% power savings respectively

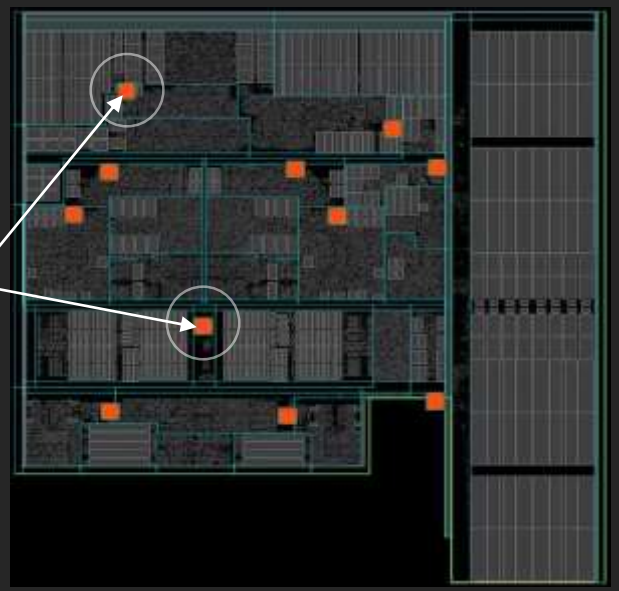


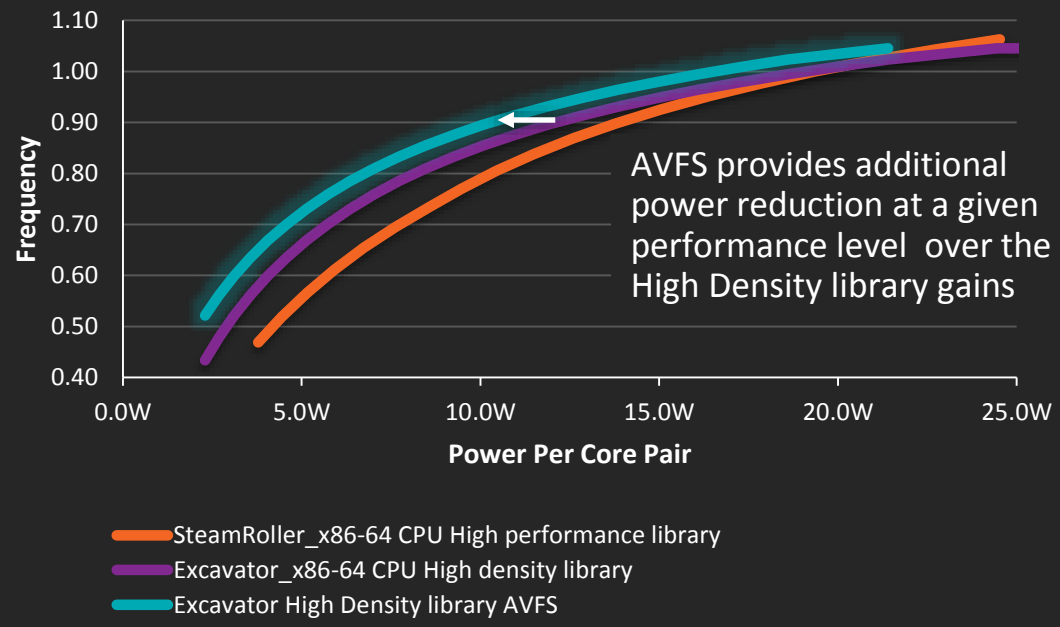


AVFS TO OPTIMIZE PERFORMANCE PER WATT

- Reliably extract the true silicon speed capability of CPU
  - Includes effects of part-to-part processing, temperature and power delivery
  - Add both a voltage and frequency sensor to existing power and temperature sensors
- Enables accurate setting of the optimal operating point for a given power or performance level across process, voltage and temperature ranges
  - Improved energy efficiency across the entire voltage/temperature operating range

"Excavator" core
incorporates
10 AVFS modules
containing
~500 frequency
sensing paths

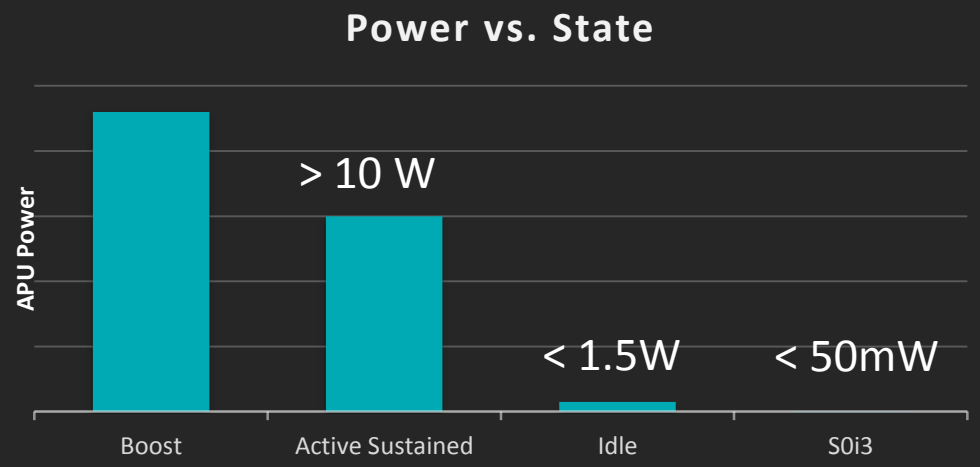


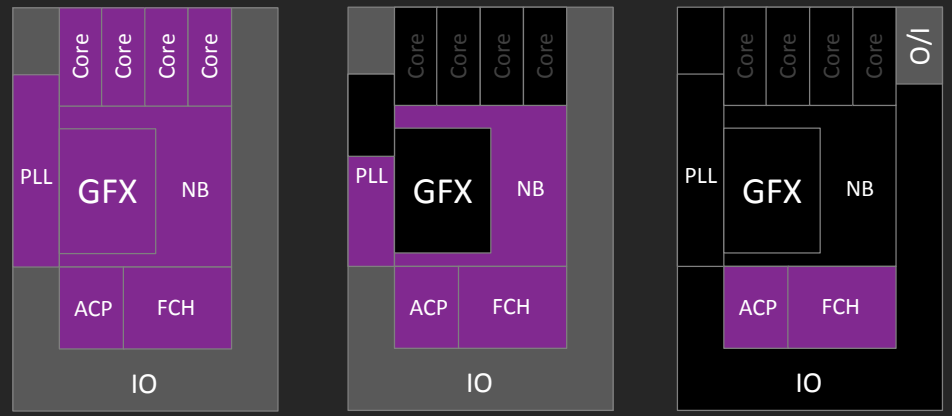


RUN-TIME ACCESS TO LOW POWER STANDBY STATE

- The S0i3 state achieves the same power level as the legacy S3 state, traditionally known as “standby” which is very time-consuming to enter and exit because it requires operating system intervention.
  - This state has almost all of the APU silicon power-gated and all relevant I/O devices in their low-power states, driving platform power to extremely low levels.
- By enabling access to this state on the fly, under the control of power management, the APU can achieve standby equivalent power levels transparently at sub-second time frames

➔ Lower average power consumption for typical use conditions.





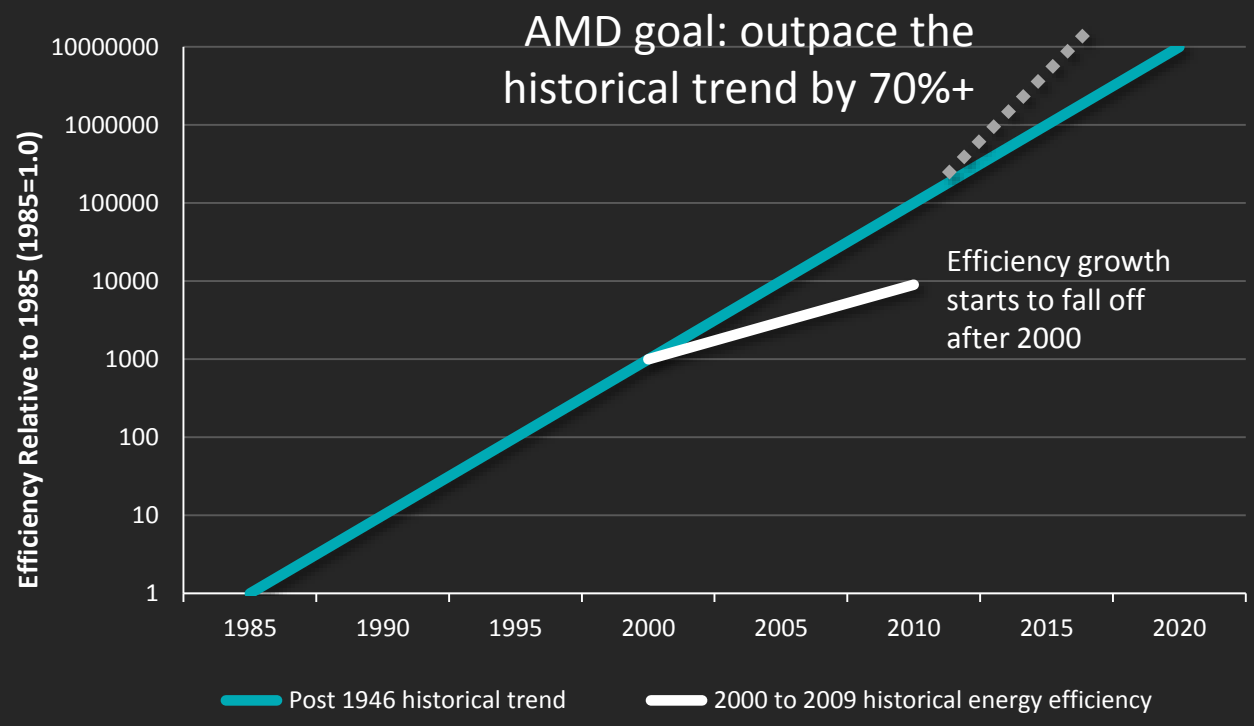
DRAMATIC IMPROVEMENTS IN ENERGY EFFICIENCY

GOAL BY 2020

IMPROVE ENERGY EFFICIENCY
for AMD mobile platforms

by at least
25 TIMES[2]

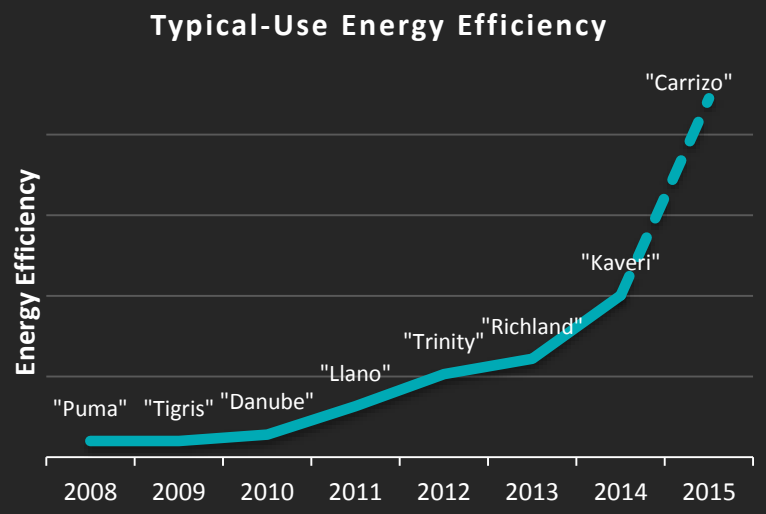
TRENDS IN THE ENERGY EFFICIENCY OF COMPUTATION[1]

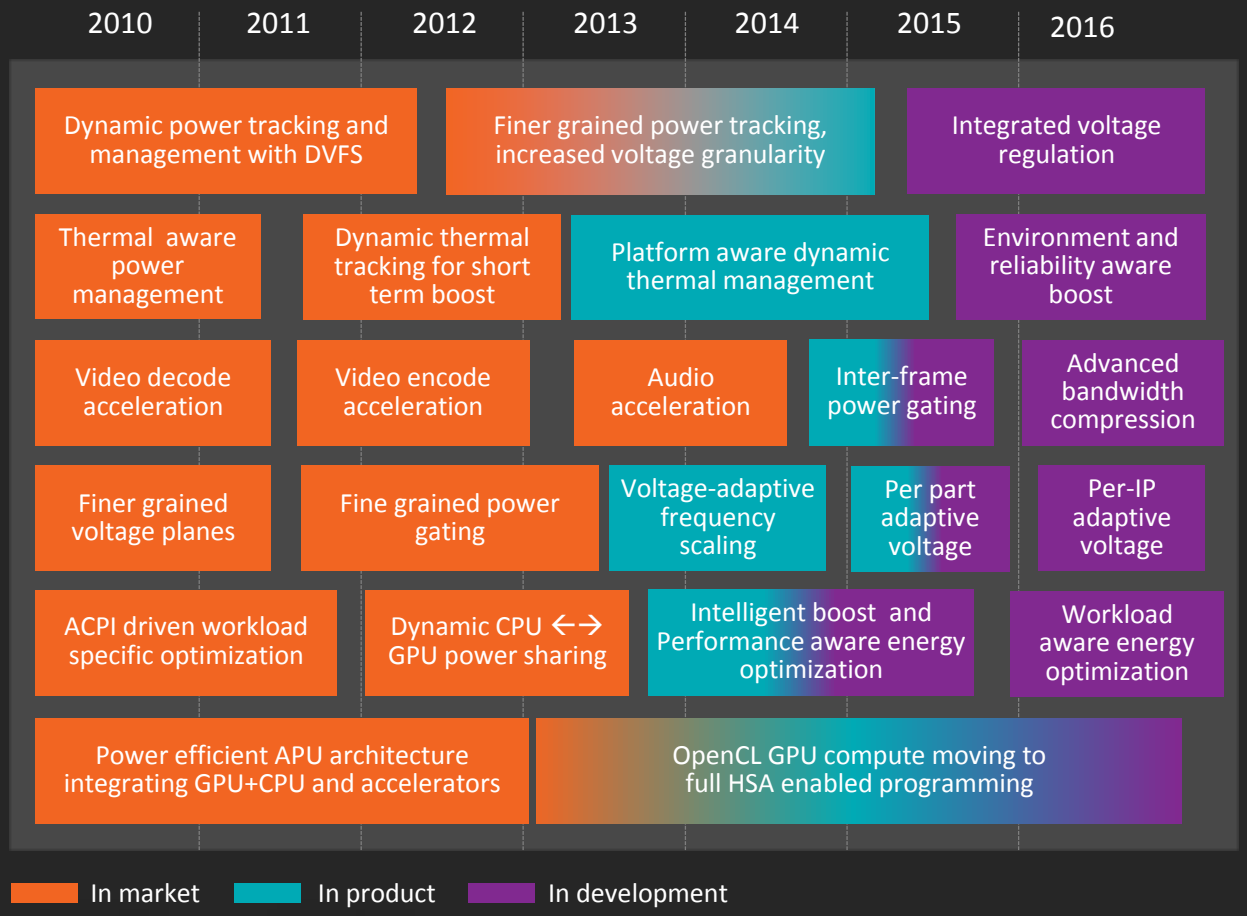


Energy use drops ↓ **While performance increases** ↑ **= Increased efficiency** +

“CARRIZO” TAPS INTO A DEEP PIPELINE OF IMPROVEMENTS

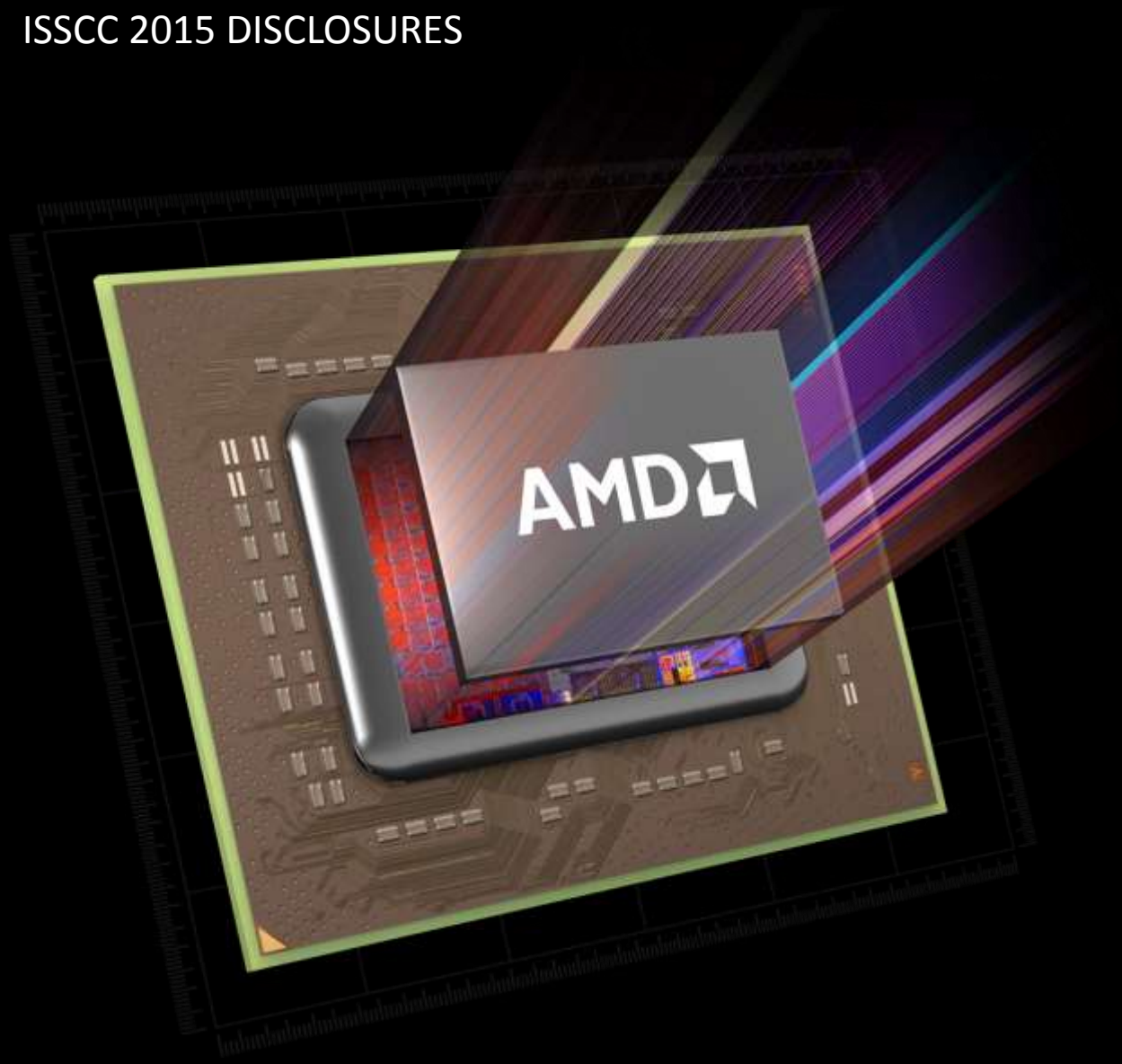
- AMD has been building a pipeline of power focused IP for many years
- Watch for more leading edge innovations enabling accelerated power gains in the future on all product lines





NEW PERFORMANCE MOBILE APU – “CARRIZO”

ISSCC 2015 DISCLOSURES



A 28NM X86 APU OPTIMIZED FOR POWER AND AREA EFFICIENCY – SESSION 4.8*

- High density design library resulting in 29% more transistors than “Kaveri” in approximately the same die area
  - 3.1 billion transistors
- Excavator cores: 5% more IPC at 40% less power and 23% less area
- H.265 support and > 3.5x transcode performance of “Kaveri”
- Separate GPU power supply rail allows eight AMD Radeon™ cores to operate more efficiently than six on “Kaveri”
- Double digit increases in performance and battery life

*A 28nm x86 APU Optimized for Power and Area Efficiency , presented by Kathryn Wilcox. Session 4.8, *Solid-State Circuits Conference Digest of Technical Papers (ISSCC).* 2015 ISSCC Conference, February, 2015.

ENDNOTES

[1] Koomey, Jonathan G., Stephen Berard, Marla Sanchez, and Henry Wong. 2011. "Implications of Historical Trends in The Electrical Efficiency of Computing." IEEE Annals of the History of Computing. vol. 33, no. 3. July-September. pp. 46-54. [http://doi.ieeecomputersociety.org/10.1109/MAHC.2010.28]

[2] Typical-use Energy Efficiency as defined by taking the ratio of compute capability as measured by common performance measures such as SpecIntRate, PassMark and PCMark®, divided by typical energy use as defined by E_{TEC} (Typical Energy Consumption for notebook computers) as specified in Energy Star Program Requirements Rev 6.0 10/2013

ATTRIBUTIONS